CLAIMS

1. A backup circuit disposed between a digital circuit (20) including a storage circuit and a power supply terminal (T_{IN}, T_{GND}) for supplying power to said digital circuit, and including a backup capacitor (C1) for supplying a backup voltage to said digital circuit when the power is cut off, thereby holding information stored in said storage circuit,

wherein said backup circuit includes devices (MOS1, MOS2) which are capable of being formed by a standard CMOS process, which are disposed between said power supply terminal (T_{IN}, T_{GND}) and said backup capacitor (C1), and which serve as resistors when the power is normally supplied to said power supply terminal, and as diodes each operating with a backward direction thereof defined as the direction from said digital circuit toward said power supply terminal when the power is cut off.

2. The backup circuit according to Claim 1,

wherein said devices are MOS transistors (MOS1, MOS2), and

gate terminals (G1, G2) of said MOS transistors are connected to a ground potential.

3. The backup circuit according to Claim 2,

wherein said MOS transistors (MOS1, MOS2) are connected in series in plural number.

4. The backup circuit according to Claim 1, further comprising:

shift means (12) for shifting said digital circuit to a power low-consumption state when a voltage at said power supply terminal drops to a level not higher than a predetermined voltage.

5. The backup circuit according to Claim 4,

wherein said shift means (12) is voltage detecting means for detecting the voltage at said power supply terminal and shifting said digital circuit to a standby state when the voltage at said power supply terminal drops to a level not higher than the predetermined voltage.

6. The backup circuit according to Claim 4,

wherein said shift means (12) is an oscillator driven by the voltage supplied from said power supply terminal, driving said digital circuit with a clock signal outputted from said oscillator, and stopping oscillation when the voltage supplied from said power supply terminal drops to a predetermined voltage.

7. The backup circuit according to Claim 1, further comprising:

reset means (14) for resetting said digital circuit when a voltage at said power supply terminal drops to a level not higher than a predetermined voltage.

8. The backup circuit according to Claim 7, wherein said reset means (14) resets said digital circuit with a delay of a predetermined time after the voltage at said power supply terminal has dropped to a level not higher than the predetermined voltage.